YAKUN SOPHIA SHAO

Research Scientist at NVIDIA
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EDUCATION

Harvard University, Cambridge, MA — Sept 2009 - May 2016
Ph.D. Candidate in Computer Science. Advisor: Professor David Brooks

Harvard University, Cambridge, MA — Sept 2009 - March 2014
Master of Science in Computer Science. Advisor: Professor David Brooks

Zhejiang University, Hangzhou, Zhejiang, China — Sept 2005 - Jun 2009
Bachelor of Electrical Engineering

BOOK

Research Infrastructures for Hardware Accelerators [Link]
Yakun Sophia Shao and David Brooks
Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers, Nov 2015.

PUBLICATIONS

Google Scholar

A Modular Digital VLSI Flow for High-Productivity SoC Design
Brucek Khailany, Matthew Fojtik, Alicia Klinefelter, Evgeni Krimer, Michael Pellauer, Nathaniel Pinckney, Haoxing Ren, **Yakun Sophia Shao**, Rangharajan Venkatesan, Yanqing Zhang, Brian Zimmer
In *Government Microcircuit Applications & Critical Technology (GOMACTech) Conference*, March 2018.

Stitch-X: An Accelerator Architecture for Exploiting Unstructured Sparsity in Deep Neural Networks [PDF]
Ching-En Lee, **Yakun Sophia Shao**, Jie-Fang Zhang, Angshuman Parashar, Joel Emer, Stephen W. Keckler, Zhengya Zhang
In *SysML Conference*, February 2018.

Using Dynamic Dependence Analysis to Improve the Quality of High-Level Synthesis Designs [PDF]
Rafael Garibotti, Brandon Reagen, **Yakun Sophia Shao**, Gu-Yeon Wei and David Brooks
In *International Symposium on Circuits and Systems (ISCAS)*, May 2017.

Co-Designing Accelerators and SoC Interfaces using gem5-Aladdin [PDF]
Yakun Sophia Shao, Sam Xi, Viji Srinivasan, Gu-Yeon Wei and David Brooks
In *International Symposium on Microarchitecture (MICRO)*, October 2016.

Design and Modeling of Specialized Architectures [PDF]
Yakun Sophia Shao
In *Ph.D. Dissertation*, Harvard University, May 2016.

The Aladdin Approach to Accelerator Design and Modeling [PDF]
Yakun Sophia Shao, Brandon Reagen, Gu-Yeon Wei and David Brooks
In *IEEE Micro*, May-June 2015.

Toward Cache-Friendly Hardware Accelerators [PDF]
Yakun Sophia Shao, Sam Xi, Viji Srinivasan, Gu-Yeon Wei and David Brooks
In *HPCA Sensors and Cloud Architectures Workshop (SCAW)*, Feb 2015.

MachSuite: Benchmarks for Accelerator Design and Customized Architectures [PDF]
Brandon Reagen, Bob Adolf, **Yakun Sophia Shao**, Gu-Yeon Wei and David Brooks
In *International Symposium on Workload Characterization (IISWC)*, Sept 2014.

Aladdin: A Pre-RTL, Power-Performance Accelerator Simulator Enabling Large Design Space Exploration of Customized Architectures [PDF]
Yakun Sophia Shao, Brandon Reagen, Gu-Yeon Wei and David Brooks
In *International Symposium on Computer Architecture (ISCA)*, June 2014.
Selected as one of the Top Picks in Computer Architecture in 2014

Energy Characterization and Instruction-Level Energy Model of Intel's Xeon Phi Processor [PDF]
Yakun Sophia Shao and David Brooks
In *International Symposium on Low Power Electronics and Design (ISLPED)*, Sept 2013.

Quantifying Acceleration: Power/Performance Trade-offs of Application Kernels in Hardware [PDF]
Brandon Reagen, **Yakun Sophia Shao**, Gu-Yeon Wei and David Brooks
In *International Symposium on Low Power Electronics and Design (ISLPED)*, Sept 2013.

ISA-Independent Workload Characterization and its Implications for Specialized Architectures [PDF]
Yakun Sophia Shao and David Brooks
In *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2013.

Power, Performance and Portability: System Design Considerations for Micro Air Vehicle Applications [PDF]
Yakun Sophia Shao, Judson Porter, Michael J. Lyons, Gu-Yeon Wei and David Brooks
In *Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)*, July 2010

AWARDS AND HONORS

- **Harvard nominee, ACM Doctoral Dissertation Award**, 2017
- **IBM Ph.D. Fellowship**, 2015-2016
- Paper selected as one of the **IEEE Micro's Top Picks in Computer Architecture** in 2014
- **Siebel Scholar, Class of 2015** - awarded annually for academic excellence and demonstrated leadership to 85 top students from the world's leading graduate schools
- **Best in Session Award**, SRC TECHCON 2014
- Invited Participant at the **Rising Stars in EECS Workshop**, 2014

SOFTWARE

- **Aladdin**: A pre-RTL, power-performance-area simulator for fixed-function accelerators. **[GitHub]**
- **gem5-Aladdin**: An SoC simulator. **[GitHub] [Users Group]**
- **LLVM-Tracer**: An LLVM optimization pass to print a dynamic LLVM IR trace. **[GitHub]**
- **MachSuite**: A benchmark suite for accelerators. **[GitHub]**
- **WIICA**: An ISA-independent workload characterization to for accelerators. **[GitHub]**

TUTORIALS

Rapid Exploration of Accelerator-Rich Architectures: Automation from Concept to Prototyping,
Yakun Sophia Shao with David Brooks, Jason Cong, Zhenman Fang, Gu-Yeon Wei and Sam Xi
In *International Symposium on Microarchitecture (MICRO)*, October 2016.

Aladdin and gem5-Aladdin: Research Infrastructures for Specialized Architectures,
Yakun Sophia Shao with David Brooks, Gu-Yeon Wei and Sam Xi
In *International Symposium on Workload Characterization (IISWC)*, September 2016.

Rapid Exploration of Accelerator-Rich Architectures: Automation from Concept to Prototyping,
Yakun Sophia Shao with David Brooks, Yu-Ting Chen, Jason Cong, Zhenman Fang, Brandon Reagen, Glenn Reinman, Gu-Yeon Wei and Sam Xi

In *International Symposium on Computer Architecture (ISCA)*, June 2015.

Research Infrastructures for Accelerator-centric Architectures,
Yakun Sophia Shao with David Brooks, Mark Hempstead, Brandon Reagen and Gu-Yeon Wei
In *International Symposium on High Performance Computer Architecture (HPCA)*, Feb 2015.

Research Infrastructures for Accelerator-centric Architectures,
Yakun Sophia Shao with David Brooks, Brandon Reagen, Kevin Skadron, Liang Wang, and Gu-Yeon Wei
In *International Symposium on Computer Architecture (ISCA)*, June 2014.

PROFESSIONAL EXPERIENCE

Research Intern, IBM Research, Yorktown Heights, NY — July 2015 - Sept. 2015
Research Intern, IBM Research, Yorktown Heights, NY — July 2014 - Sept. 2014
Research Intern, Intel Corporation, Santa Clara, CA — June 2012 - Sept. 2012

REVIEW EXPERIENCE

Editing

- Guest Editor, IEEE Micro Special Issue on "Hardware Acceleration", November/December 2018

Technical Program Committees

- Design Automation Conference (DAC), 2018
- International Symposium on High-Performance Computer Architecture (HPCA) Industry Session, 2018
- International Symposium on Computer Architecture (ISCA), 2017

External Technical Program Committees

- International Symposium on High-Performance Computer Architecture (HPCA), 2018

Journal Reviewer

- ACM Transactions on Architecture and Code Optimization (TACO)
- IEEE Computer Architecture Letters (CAL)
- IEEE Micro
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Computers
- Microelectronics Journal
- Integration, the VLSI Journal
- International Journal of Information Technology & Decision Making

TEACHING EXPERIENCE

CS247r Advanced Topics in Computer Architecture, Fall 2013, Teaching Fellow
CS246 Advanced Computer Architecture, Spring 2013, Teaching Fellow
CS141 Computing Hardware, Fall 2011, Teaching Fellow